# 328812 (28)

## BE (8th Semester)

## Examination, April - May, 2021

## Branch : Et & T

## VLSI DESIGN

***Time Allowed : Three Hours***

***Maximum Marks : 80***

***Minimum Pass Marks : 28***

**Note :** Part (a) of each unit is compulsory. Attempt any two parts from (b), (c) and (d).

### UNIT - I

**Q. 1.** (a) What is SSI, MSI and VLSI. **2**

(b) Explain VLSI Design Flow using flow chart. **7**

(c) Explain design hierarchy concept of regularity modularity and locality. 7

(d) Write short notes on FPGA and Design $F = \bar{x}_1\bar{x}_2 + x_1x_2$ using two input LUT. 7

## UNIT - II

Q. 2. (a) Draw the circuit diagram of CMOS inverter. 2

(b) Explain basic steps of fabrication process of CMOS. 7

(c) Design circuit diagram and layout of 3 Input NAND gate. 7

(d) Draw basic BiCMOS circuit of two input NAND gate. 7

## UNIT - III

**Q. 3.** (a) What is the difference between SRAM and DRAM. **2**

(b) Draw circuit diagram of 4 × 4 MOS NOR ROM and explain storage in each location. **7**

(c) Design schematic of 4 × 1 MUX. **7**

(d) Draw schematic and layout of 6 transistor SRAM cell. **7**

## UNIT - IV

**Q. 4.** (a) What is entity in VHDL. **2**

(b) Write short notes on process statement and write down VHDL code of 4 × 1 MUX. **7**

(c) Explain in brief structural style of modelling with one example. **7**

(d) Write VHDL code for 9 Bit Parity generator circuits. 7

## UNIT - V

Q. 5. (a) What is FSM. 2

(b) What is the difference between Melay & Moore State Machine. 7

(c) Write short note on operator overloading. 7

(d) Design an FSM that has input w and an output z. The machine is a sequence detector that produces z = 1 when the previous two values of w were 00 or 11, otherwise z = 0. 7